



## PATENT ABSTRACTS OF JAPAN

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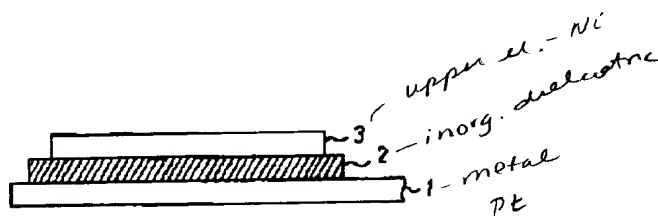
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**MIZUSAWA YUMI  
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SAITO MASAYUKI**(54) **THIN FILM CAPACITOR**

## (57) Abstract:

**PURPOSE:** To obtain a small-sized high capacity thin film capacitor by forming a metal body on a thin inorganic dielectric deposited on a metal foil.

**CONSTITUTION:** The thin film capacitor comprises a thin inorganic dielectric 2 deposited on a metal foil 1 serving as a substrate and a lower electrode, and an upper electrode, i.e., a metal body 3, formed on the thin inorganic dielectric 2. When the thin film capacitor is produced, a thin inorganic dielectric of  $(\text{Ba}_{0.5}, \text{Sr}_{0.5})\text{TiO}_3$  is deposited, as a mask, on the metal foil, i.e., a Pt foil 1, using an-RF magnetron sputtering system. A thin mask of Ni 3 is then deposited, as the metal body 3, on the thin inorganic dielectric 2 using an RF magnetron. Since the total thickness of an element is decreased, the thin inorganic dielectrics and the metal bodies can be laminated in multilayer thus realizing a small-sized high capacity thin film capacitor.



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(54) 【発明の名称】 薄膜キャパシタ

(57) 【要約】

【目的】 プロセスを複雑にすること無く小型・大容量の薄膜キャパシタを提供することを目的とする。

【構成】 金属箔体1と、金属箔体1上に成膜された無機誘電体薄膜2と、この無機誘電体薄膜2上に形成された金属体3とを具備することを特徴とする薄膜キャパシタ。



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(実施例 1) 図 1 は本発明の薄膜キャパシタの概略構成を示す断面図である。基板と下部電極を兼ねている金属箔体 1 上に成膜形成された無機誘電体薄膜 2、この無機誘電体薄膜 2 上に上部電極である金属体 3 が形成されている。

【0014】次に本実施例による薄膜キャパシタの製造方法を示す。先ず金属箔体 1 として厚さ  $10\mu\text{m}$  の Pt 箔 1 を用意し、この Pt 箔 1 上に、RF マグネトロンスパッタリング装置（株）芝浦製作所製：CFS-8EP-55SC）を用いて、 $(\text{Ba}_{0.5}\text{Sr}_{0.5})\text{TiO}_3$  無機誘電体薄膜 2 を  $200\text{nm}$  マスク成膜する。この時の成膜温度は  $500^\circ\text{C}$  とした。

【0015】次にこの無機誘電体薄膜 2 上に、RF マグネトロンスパッタリング装置により、成膜温度  $350^\circ\text{C}$  で金属体 3 として Ni 薄膜 3 を  $100\text{nm}$  マスク成膜する。上部電極のサイズは  $1\text{mm}$  角とした。

【0016】こうして得られた薄膜キャパシタの誘電特性を測定したところ、キャパシタサイズ  $1\text{mm} \times 1\text{mm} \times 10\mu\text{m}$  t に対し、静電容量  $C = 30\text{nF}$  の値が得られ良好な特性が得られた。

【0017】このキャパシタは、例えば  $0.6\text{mm}$  厚の熱酸化膜付き Si ウエハ上に作成されたキャパシタに比べて、約 60 分の 1 の薄膜化が達成されている。さらにこのキャパシタをマザーボード上に実装する際に、下部電極の導通は金属箔基板の下面を導電性ペーストにより接着することで得られるので、ワイヤボンディングで実装する場合にもボンディングパッドが 1 つ（上部電極用）だけでよい。従って周辺に要するスペースが半減するため高密度実装に適している。従って本実施例では素子の小型化に充分な大きさと充分な静電容量を得ることができる。

【0018】（実施例 2）表面仕上げ状態の異なる 4 種類の金属箔体 1 である Pt 箔 1（ $10\mu\text{m}$  厚、表面粗さ  $R_a = 1\text{nm}$ 、 $5\text{nm}$ 、 $10\text{nm}$ 、 $20\text{nm}$ ）上に、RF マグネトロンスパッタリング装置を用いて、無機誘電体薄膜 2 として  $\text{SrTiO}_3$ 、薄膜 2（膜厚  $100\text{nm}$ 、成膜温度  $500^\circ\text{C}$ ）、金属体 3 として Ni 薄膜 3（膜厚  $100\text{nm}$ 、成膜温度  $350^\circ\text{C}$ ）を順次マスクを用いて成膜した。素子のサイズは約  $1\text{mm}$  角とした。

【0019】こうして得られた薄膜キャパシタの誘電特性を測定したところ、 $\text{SrTiO}_3$  膜厚  $t$  が Pt 箔の  $R_a$  に対し、 $t \geq 20 \times R_a$  の関係を満たす場合に、リーク電流密度  $J \leq 10^{-5}\text{A}/\text{cm}^2$ 、破壊電圧  $V_{\text{max}} \geq 20\text{V}$  の実用的な値が得られた。

【0020】本実施例においても素子の小型化に充分な大きさと充分な静電容量を得ることができる。

（実施例 3）先ず金属箔体 1 として厚さ  $5\mu\text{m}$  の Al 箔 1 を用意し、この Al 箔 1 上に、RF マグネトロンスパッタリング装置を用いて、無機誘電体薄膜 2 として  $\text{SrTiO}_3$ 、薄膜 2（膜厚  $100\text{nm}$ 、成膜温度  $400^\circ\text{C}$ ）

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を  $1\text{mm} \times 100\text{mm}$  の帯状のマスクにより成膜した。

【0021】次にこの無機誘電体薄膜 2 上に、上記マスクを用いて RF マグネトロンスパッタリング装置により、金属体 3 として Ni 薄膜 3（膜厚  $100\text{nm}$ 、成膜温度  $350^\circ\text{C}$ ）を成膜した。次に Ni 箔 1 及び Ni 薄膜 3 に Pt の引き出し線（図示せず）を溶接し、 $\text{SrTiO}_3$  薄膜 2 及び Ni 薄膜 3 が積層された Ni 箔 1 を帯の短辺（ $1\text{mm}$  長）を軸として巻き込んだところ、直径約  $1\text{mm}$ 、長さ  $1\text{mm}$  の円柱状の薄膜キャパシタが完成した。

【0022】こうして得られた薄膜キャパシタの誘電特性を測定したところ、キャパシタサイズ  $1\text{mm} \phi \times 1\text{mm}$  m に対し、静電容量  $C = 4.4\mu\text{F}$  の大容量値が得られた。このキャパシタは通常の有機フィルムコンデンサと同様な巻き込み型が有機誘電体より比誘電率が 2 オーダ大きな無機高誘電率薄膜により実現しているので、同じ容量の有機フィルムコンデンサに比してキャパシタサイズを 2 オーダ小さくできる。従って本実施例では素子の小型化に充分な大きさと充分な静電容量を得ることができる。

【0023】（実施例 4）先ず金属箔体 1 として厚さ  $5\mu\text{m}$  の Ni 箔 1 を用意し、この Ni 箔 1 上に、RF マグネトロンスパッタリング装置を用いて、無機誘電体薄膜 2 として  $\text{SrTiO}_3$ 、薄膜 2（膜厚  $100\text{nm}$ 、成膜温度  $400^\circ\text{C}$ ）を  $1\text{mm} \times 50\text{mm}$  の帯状のマスクにより成膜した。

【0024】次にこの無機誘電体薄膜 2 上に、上記マスクを用いて RF マグネトロンスパッタリング装置により、金属体 3 として Ni 薄膜 3（膜厚  $100\text{nm}$ 、成膜温度  $350^\circ\text{C}$ ）を成膜した。次に Ni 箔 1 及び Ni 薄膜 3 に Pt の引き出し線（図示せず）を溶接し、 $\text{SrTiO}_3$ 、薄膜 2 及び Ni 薄膜 3 が積層された Ni 箔 1 を帯の短辺（ $1\text{mm}$  長）を軸として長辺方向を  $1\text{mm}$  幅につづら折りにしたところ、幅  $1\text{mm}$ 、長さ  $1\text{mm}$ 、厚さ約  $1\text{mm}$  の薄膜キャパシタが完成した。

【0025】こうして得られた薄膜キャパシタの誘電特性を測定したところ、キャパシタサイズ  $1\text{mm} \times 1\text{mm} \times 1\text{mm}$  に対し、静電容量  $C = 1.1\mu\text{F}$  の大容量値が得られた。本実施例においても実施例 3 と同様な理由により、素子の小型化に充分な大きさと充分な静電容量を得ることができる。

【0026】（実施例 5）図 2（a）、（b）、（c）は本実施例に係る薄膜キャパシタの製造工程を説明する断面図である。

【0027】先ず図 2（a）に示すように、金属箔体 4 として厚さ  $5\mu\text{m}$  の Pt 箔 4 を用意し、この Pt 箔 4 上に、RF マグネトロンスパッタリング装置を用いて、無機誘電体薄膜 5 として  $(\text{Ba}_{0.5}\text{Sr}_{0.5})\text{TiO}_3$ 、薄膜 5（膜厚  $200\text{nm}$ 、成膜温度  $500^\circ\text{C}$ ）及び金属体 6 として Pt 薄膜 6（膜厚  $50\text{nm}$ 、成膜温度  $400^\circ\text{C}$ ）

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て)をそれぞれ無機誘電体薄膜5を4層、金属体6を3層、計7層を順次成膜した。その際、(Ba<sub>0.5</sub>Sr<sub>0.5</sub>)TiO<sub>3</sub>薄膜5が図中に示すように互い違いに接触するようにPt薄膜6をマスク成膜した。

【0028】次に図2(b)に示すように、PEP工程、イオンミリング工程、レジスト剥離工程により、(Ba<sub>0.5</sub>Sr<sub>0.5</sub>)TiO<sub>3</sub>薄膜5及びPt薄膜6の両側を一括テーパーエッチングした。その際、図中に示すように無機誘電体薄膜層5の最下層の片側が残るように、エッチング途中にPEP工程を挟んで行った。

【0029】次に図2(c)に示すように、Ni電極層7a及び7bを形成した。その結果、Ni電極7aとPt電極層6aとPt箔4とが電気的に接触し、Ni電極層7aとPt電極6bとが電気的に接触した構造となり、無機誘電体層5を介して電極層が重なっている部分(図中L)が多層のキャパシタの構成となる。

【0030】こうして得られた薄膜キャパシタの誘電特性を測定したところ、キャパシタサイズ1mm×1mm×6μmに対し、静電容量C=120nFの値が得られた。

【0031】このキャパシタは通常の例えば0.6mm厚熱酸化膜付きSi上に作成した同構造のキャパシタに比べて、約100分の1の薄膜化が達成されている。従って本実施例では素子の小型化に充分な大きさで充分な静電容量を得ることができる。

【0032】(実施例6)図3は本発明の薄膜キャパシタを使用した移動体通信端末のパワーアンプモジュールの一部を示す断面図であり、図中8はAl<sub>2</sub>O<sub>3</sub>基板、9は金属箔体であるPt箔、10は無機誘電体薄膜であるSrTiO<sub>3</sub>薄膜、11は金属体であるNi薄膜、12はポリイミド絶縁膜、13はNi電極、14は半田バンプ、8はICを組み込んだ半導体素子をそれぞれ示している。

【0033】次にこの装置の製造方法を説明する。まず厚さ5μmのPt箔9上にSrTiO<sub>3</sub>薄膜10と第1のNi薄膜11をそれぞれ100nm毎RFマグネトロンスパッタ成膜し、PEP工程、Niエッチング、レジスト剥離処理を経て100μm角の薄膜キャパシタを形成した。

【0034】次にこの薄膜キャパシタをダイシングして200μm角に切り出して、Al<sub>2</sub>O<sub>3</sub>基板8上に導電ペーストで接着した後、Al<sub>2</sub>O<sub>3</sub>基板8上にポリイミドを塗布、露光現像処理を施してポリイミド絶縁膜12を20μm厚形成した。

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\*【0035】次に第2のNi薄膜13を2μm厚蒸着し、このNi薄膜13上にPEP工程によりポリイミド絶縁膜12と同じパターンでレジスト(図示せず)を8μm厚にパターン形成した。

【0036】次に前記レジストをマスクとし、第2のNi膜13をカソード層として、めっき法により半田を積層後、前記レジストを除去し100μm角、高さ30μmの半田バンプ14を4個形成した。

【0037】次にこの4個の半田バンプ14が半導体素子15の四隅と一致するように、半導体素子15を配置し半田リフローにより、半導体素子15を実装した。本実施例のように、金属箔体を用いた薄膜キャパシタは素子全体の厚みをバンプの高さに比べると十分に薄く構成できるので、バンプとパッド間に本発明による薄膜キャパシタを介在させることが可能となり高密度実装を実現できる。

【0038】

【発明の効果】以上説明したように、本発明によれば素子全体の厚みが飛躍的に減少し、また巻き込み・折り畳みによる多層化、無機誘電体薄膜と金属体を交互に積層することによる多層化が可能であるので、小型・大容量の薄膜キャパシタを提供することができる。

【図面の簡単な説明】

【図1】 本発明による薄膜キャパシタの断面図。

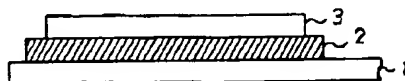
【図2】 本発明による薄膜キャパシタの製造方法を説明する断面図。

【図3】 本発明による薄膜キャパシタを半導体チップと基板間に介在して構成した装置の断面図。

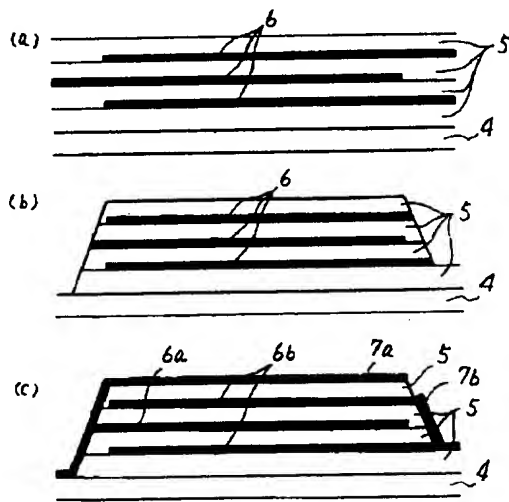
【符号の説明】

- 1・・・金属箔体
- 2・・・無機誘電体薄膜
- 3・・・金属体
- 4・・・金属箔体
- 5・・・無機誘電体薄膜
- 6・・・金属体
- 7・・・電極
- 8・・・Al<sub>2</sub>O<sub>3</sub>基板
- 9・・・金属箔体
- 10・・・無機誘電体薄膜
- 11・・・金属体
- 12・・・ポリイミド絶縁膜
- 13・・・Ni電極
- 14・・・半田バンプ
- 15・・・半導体素子

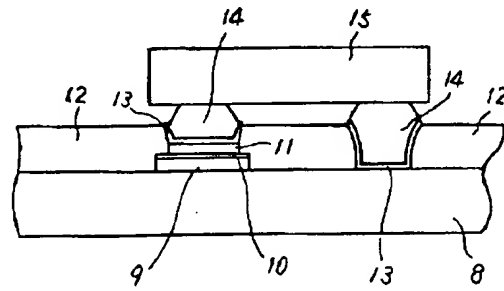
【図1】



【図 2】



【図 3】



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## DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Industrial Application] this invention relates to the thin film capacitor used for a multi chip module (MCM), the circuit module for mobile telecom terminals, etc.

[0002]

[Description of the Prior Art] Further miniaturization and high-density-assembly-ization of mounting technology are demanded with a miniaturization, improvement in the speed, and highly-efficient-izing of an electron device. Miniaturization and high-density-assembly-ization have been advanced also for capacitor parts, such as a decoupling capacitor for power supply stable carried in a circuit module in such a demand. Although capacitor parts had the chip conventionally in use, the thin film capacitor is examined as a method of a chip having a limitation pointed out by the miniaturization and replacing with this.

[0003] The thin film capacitor has constituted the structure where the conductive thin film which is a lower electrode, the inorganic-dielectric film, and the conductor film which is an up electrode were formed one by one on the substrate which is a base material, and the creation is usually performed by performing the membrane formation process by vacuum evaporation, sputtering, etc., and the patterning process by PEP and etching repeatedly to each class.

[0004] As a merit to the chip of a thin film capacitor, two points of large-capacity-izing accompanying the miniaturization by sharp reduction of (1) each thickness and thin-film-izing of (2) inorganic-dielectric layers are gained. However, since the substrate which is a base material is required for thin film creation, it has a limitation also in a miniaturization and large capacity-ization for the multilayering seen by chips, such as a film capacitor, to be difficult etc. from the complexity of that thickness of the whole element cannot be made below into the thickness of a substrate, and a creation process which was mentioned above.

[0005]

[Problem(s) to be Solved by the Invention] As mentioned above, the present condition is that small [ required for a miniaturization and improvement in the speed ] and the mass thin film capacitor of a device are not offered. this invention is accomplished in view of the above-mentioned trouble, and it aims at offering small and a mass thin film capacitor, without complicating a process.

[0006]

[Means for Solving the Problem] In order to solve the above-mentioned trouble, the thin film capacitor by the invention in this application is characterized by providing a metallic foil object, the inorganic-dielectric thin film formed on the metallic foil object, and the metal body formed on the aforementioned inorganic-dielectric thin film.

[0007] Moreover, the thin film capacitor by this invention is characterized by being involved in or being collapsed. Thickness is the metal plate of micron order and 5-100 micrometers of board thickness of the aforementioned metallic foil object are desirable. Especially if conductivity is shown as a metallic foil object material and it is with a high material of opportunity-ductility and malleability, although it will not be limited, Pd, Au, aluminum, nickel, and Pt are desirable. moreover, SrTiO<sub>3</sub> later mentioned as an inorganic-dielectric thin film material and BaSrTiO<sub>3</sub> etc. -- when using oxide ceramics, especially noble metals, such as Pt, Au, and Pd, are desirable at the point of not making a resultant with a low dielectric constant to the interface of a metallic foil object and an inorganic-dielectric thin film layer

[0008] as an inorganic-dielectric thin film material -- SiO<sub>2</sub>, Ta<sub>2</sub>O<sub>3</sub>, SrTiO<sub>3</sub>, and BaSrTiO<sub>3</sub> although it begins and thin-film-izing is possible, and it will not be limited especially if it is -- 2 receive 2 or more figure of SiO(s), and Ta<sub>2</sub>O<sub>3</sub> SrTiO<sub>3</sub> which receives and has a dielectric constant big 1 or more figures, and BaSrTiO<sub>3</sub> etc. -- the oxidization ceramics which have a perovskite structure are more desirable in respect of large-capacity-izing

[0009] Moreover, Pt, Au, Pd, nickel, aluminum, etc. are desirable at the reason same as a metal-body material as metallic foil object material. Especially the membrane formation method of an inorganic-dielectric thin film and a metal body is not limited, but may be based on wet methods, such as anodic oxidation besides vacuum processes, such as vacuum evaporation and sputtering, and a sol-gel method. If the forming-membranes method in which mask membrane formation is possible is used like vacuum evaporation and sputtering, a PEP process can be cut down and facilitation of a process can be attained.

[0010] moreover -- as an inorganic-dielectric thin film -- SrTiO<sub>3</sub> and BaSrTiO<sub>3</sub> etc. -- since it is obtained that a film [ carry / in vacuum processes, such as vacuum evaporation and sputtering, ] is more nearly quality when using the oxidization ceramics which have a perovskite structure, it is more desirable

[0011] In this invention, multilayering becomes possible as a metallic foil object by bending, such as Pt, Au, Pd, nickel, and aluminum, contamination, folding by using a strong material distorted, etc. In multilayering by contamination, folding, etc., in order to avoid the electric contact to a metallic foil object and a metal body if needed, it is effective to form the insulator on a thin film on the aforementioned metal body. Moreover, it is also effective to attain multilayering by making it the multilayer structure which carried out the laminating of the conductor thin film to the aforementioned inorganic-dielectric thin film by turns as a metal

body besides contamination and fold

[0012]

[Function] this invention serves as the metallic foil object as the substrate which makes an inorganic-dielectric thin film form, and an electrode. the thickness of the whole element decreases by leaps and bounds by carrying out like this -- natural -- further -- contamination - collapsing -- etc. -- it becomes possible to realize the miniaturization of an element

[0013]

[Example] With reference to a drawing, the example of this invention is explained in detail below.

(Example 1) Drawing 1 is the cross section showing the outline composition of the thin film capacitor of this invention. The metal body 3 which is an up electrode is formed the inorganic-dielectric thin film 2 by which membrane formation formation was carried out on the metallic foil object 1 which serves both as the substrate and the lower electrode, and on this inorganic-dielectric thin film 2.

[0014] Next, the manufacture method of the thin film capacitor by this example is shown. The Pt foil 1 with a thickness of 10 micrometers is first prepared as a metallic foil object 1, RF magnetron sputtering system (Shibaura Engineering Works Co., Ltd. make : CFS-8EP-55SC) is used on this Pt foil 1, and it is TiO (Ba0.5 Sr0.5)3. 200nm mask membrane formation of the inorganic-dielectric thin film 2 is carried out. Membrane formation temperature at this time was made into 500 degrees C.

[0015] Next, on this inorganic-dielectric thin film 2, 100nm mask membrane formation of the nickel thin film 3 is carried out as a metal body 3 at the membrane formation temperature of 350 degrees C by RF magnetron sputtering system. Size of an up electrode was used as 1mm angle.

[0016] In this way, when the dielectric characteristics of the obtained thin film capacitor were measured, it is capacitor size 1mmx1mmx10micromt. It received, the value of electrostatic-capacity  $C=30nF$  was acquired, and the good property was acquired.

[0017] Thin film-ization of about 1/60 is attained compared with the capacitor with which this capacitor was created on Si wafer with a thermal oxidation film of for example, 0.6mm \*\*. Since the flow of a lower electrode is obtained by pasting up the undersurface of a metallic foil substrate with a conductive paste in case this capacitor is furthermore mounted on a mother board, when it mounts by wirebonding, the number of bonding pads is one sufficient (for up electrodes). Therefore, since the space required on the outskirts is halved, it is suitable for high density assembly. Therefore, electrostatic capacity sufficient in size sufficient in this example for the miniaturization of an element can be obtained.

[0018] (Example 2) The Pt foil 1 (it \*\* 10 micrometers) which are four kinds of metallic foil objects 1 with which surface-finish states differ RF magnetron sputtering system is used on surface roughness  $Ra=1nm, 5nm, 10nm, \text{ and } 20nm$ . It is  $SrTiO_3$  as an inorganic-dielectric thin film 2. The nickel thin film 3 (thickness of 100nm, membrane formation temperature of 350 degrees C) was formed one by one, using a mask as a thin film 2 (thickness of 100nm, membrane formation temperature of 500 degrees C), and a metal body 3. Size of an element was used as about 1mm angle.

[0019] In this way, when the dielectric characteristics of the obtained thin film capacitor were measured and the  $SrTiO_3$  thickness t filled the relation of  $t \geq 20 \times Ra$  to  $Ra$  of Pt foil, leakage-current density  $J \leq 10^{-5} A/cm^2$  and the practical value of breakdown voltage  $V_{max} \geq 20V$  were acquired.

[0020] Also in this example, sufficient electrostatic capacity can be obtained in sufficient size for the miniaturization of an element.

(Example 3) The aluminum foil 1 with a thickness of 5 micrometers is first prepared as a metallic foil object 1, RF magnetron sputtering system is used on this aluminum foil 1, and it is  $SrTiO_3$  as an inorganic-dielectric thin film 2. The thin film 2 (thickness of 100nm, membrane formation temperature of 400 degrees C) was formed with the 1mmx100mm band-like mask.

[0021] Next, on this inorganic-dielectric thin film 2, the above-mentioned mask was used and the nickel thin film 3 (thickness of 100nm, membrane formation temperature of 350 degrees C) was formed as a metal body 3 by RF magnetron sputtering system. Next, the outgoing line (not shown) of Pt is welded to the nickel foil 1 and the nickel thin film 3, and it is  $SrTiO_3$ . When the thin film 2 and the nickel thin film 3 involved in the nickel foil 1 by which the laminating was carried out centering on the shorter side (1mm length) of a band, the thin film capacitor of the shape of a pillar with a diameter [ of about 1mm ] and a length of 1mm was completed.

[0022] In this way, when the dielectric characteristics of the obtained thin film capacitor were measured, the mass value with an electrostatic capacity of  $C=4.4 \text{ micro F}$  was acquired to capacitor size 1mmx1mm. the contamination type as the usual organic film capacitor with this same capacitor -- an organic dielectric -- specific inductive capacity -- 2 order size -- since the \*\*\*\* inorganic quantity dielectric constant thin film has realized, as compared with the organic film capacitor of the same capacity, capacitor size can be made small 2 order Therefore, electrostatic capacity sufficient in size sufficient in this example for the miniaturization of an element can be obtained.

[0023] (Example 4) The nickel foil 1 with a thickness of 5 micrometers is first prepared as a metallic foil object 1, RF magnetron sputtering system is used on this nickel foil 1, and it is  $SrTiO_3$  as an inorganic-dielectric thin film 2. The thin film 2 (thickness of 100nm, membrane formation temperature of 400 degrees C) was formed with the 1mmx50mm band-like mask.

[0024] Next, on this inorganic-dielectric thin film 2, the above-mentioned mask was used and the nickel thin film 3 (thickness of 100nm, membrane formation temperature of 350 degrees C) was formed as a metal body 3 by RF magnetron sputtering system. Next, the outgoing line (not shown) of Pt is welded to the nickel foil 1 and the nickel thin film 3, and it is  $SrTiO_3$ . When the direction of the long side was made into 1mm width of face centering on the shorter side (1mm length) of a band at the winding path, the thin film capacitor with width of face of 1mm, a length [ of 1mm ], and a thickness of about 1mm completed the nickel foil 1 with which the laminating of a thin film 2 and the nickel thin film 3 was

[0025] In this way, when the dielectric characteristics of the obtained thin film capacitor were measured, the mass value with an electrostatic capacity of  $C=1.1 \text{ micro F}$  was acquired to capacitor size 1mmx1mmx1mm. Also in this example, sufficient electrostatic capacity can be obtained in sufficient size for the miniaturization of an element for the same reason as an example 3.

[0026] (Example 5) Drawing 2 (a), (b), and (c) are the cross sections explaining the manufacturing process of the thin film

capacitor concerning this example.

[0027] As first shown in drawing 2 (a), the Pt foil 4 with a thickness of 5 micrometers is prepared as a metallic foil object 4. RF magnetron sputtering system is used on this Pt foil 4. It is  $\text{TiO}_3$  as an inorganic-dielectric thin film 5 ( $\text{Ba}_{0.5}\text{Sr}_{0.5}$ ). As a thin film 5 (thickness of 200nm, membrane formation temperature of 500 degrees C), and a metal body 6, the inorganic-dielectric thin film 5 was formed for the Pt thin film 6 (thickness of 50nm, membrane formation temperature of 400 degrees C), and three layers and a total of seven layers were formed for four layers and the metal body 6 one by one, respectively. It is  $\text{TiO}(\text{Ba}_{0.5}\text{Sr}_{0.5})_3$  in that case. Mask membrane formation of the Pt thin film 6 was carried out so that it might contact alternately, as a thin film 5 showed all over drawing.

[0028] Next, as shown in drawing 2 (b), it is  $\text{TiO}(\text{Ba}_{0.5}\text{Sr}_{0.5})_3$  by the PEP process, the ion milling process, and the resist exfoliation process. Package taper etching of the both sides of a thin film 5 and the Pt thin film 6 was carried out. At that time, the PEP process was inserted in the middle of etching so that one side of the lowest layer of the inorganic-dielectric thin film layer 5 might remain, as shown all over drawing.

[0029] Next, as shown in drawing 2 (c), nickel electrode layers 7a and 7b were formed. Consequently, nickel electrode 7a, Pt electrode layer 6a, and the Pt foil 4 serve as structure which was contacted electrically and nickel electrode layer 7a and Pt electrode 6b contacted electrically, and the portion (inside L of drawing) with which the electrode layer has lapped through the inorganic-dielectric layer 5 serves as composition of a multilayer capacitor.

[0030] In this way, when the dielectric characteristics of the obtained thin film capacitor were measured, it is capacitor size  $1\text{mm} \times 1\text{mm} \times 6\text{micromt}$ . It received and the value of electrostatic-capacity  $C=120\text{nF}$  was acquired.

[0031] Thin film-ization of about 1/100 is attained compared with the capacitor of this structure which created this capacitor for example, on usual Si with 0.6mm thick thermal oxidation film. Therefore, electrostatic capacity sufficient in size sufficient in this example for the miniaturization of an element can be obtained.

[0032] (Example 6) Drawing 3 is the cross section showing some power amplification modules of the mobile telecom terminal which used the thin film capacitor of this invention, and eight in drawing is aluminum 2O3. 10 is a substrate, Pt foil whose 9 is a metallic foil object, and  $\text{SrTiO}_3$  which is an inorganic-dielectric thin film. A thin film, nickel thin film whose 11 is a metal body, and 12 show the semiconductor device in which nickel thin film and 14 included the solder bump, and; as for a polyimide insulator layer and 13, 8 included IC, respectively.

[0033] Next, the manufacture method of this equipment is explained. It is  $\text{SrTiO}_3$  on the Pt foil 9 with a thickness of 5 micrometers first. RF magnetron-sputtering membrane formation of a thin film 10 and the 1st nickel thin film 11 was carried out the whole 100nm, respectively, and the thin film capacitor of 100-micrometer angle was formed through a PEP process, nickel etching, and resist exfoliation processing.

[0034] Next, the dicing of this thin film capacitor is carried out, and it starts on 200-micrometer square, and is aluminum 2O3. aluminum 2O3 after pasting up with an electric conduction paste on a substrate 8 On the substrate 8, the application and the exposure development were given for the polyimide and the polyimide insulator layer 12 was 20 micrometer-thick-formed.

[0035] Next, 2-micrometer thick vacuum evaporatio of the 2nd nickel thin film 13 was carried out, and pattern formation of the resist (not shown) was carried out to 8-micrometer \*\* by the same pattern as the polyimide insulator layer 12 according to the PEP process on this nickel thin film 13.

[0036] Next, the aforementioned resist was used as the mask, after a laminating and the aforementioned resist were removed for solder by the galvanizing method by having used the 2nd nickel film 13 as the cathode layer, and 100-micrometer angle and the solder bump 14 with a height of 30 micrometers were formed four pieces.

[0037] Next, the semiconductor device 15 has been arranged and the semiconductor device 15 was mounted by the solder reflow so that this four solder bump 14 might be in agreement with the four corners of a semiconductor device 15. Like this example, since the thin film capacitor using the metallic foil object can constitute the thickness of the whole element thinly enough compared with a bump's height, it becomes possible to make the thin film capacitor by this invention intervene between pads with a bump, and high density assembly can be realized.

[0038]

[Effect of the Invention] Since the multilayering by the thickness of the whole element decreasing by leaps and bounds, and carrying out the laminating of the metal body to the multilayering by contamination and folding and an inorganic-dielectric thin film by turns is possible according to this invention as explained above, small and a mass thin film capacitor can be offered.

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#### DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] The cross section of the thin film capacitor by this invention.

[Drawing 2] The cross section explaining the manufacture method of the thin film capacitor by this invention.

[Drawing 3] The cross section of the equipment which intervened between the semiconductor chip and the substrate and constituted the thin film capacitor by this invention.

[Description of Notations]

- 1 ... Metallic foil object
- 2 ... Inorganic-dielectric thin film
- 3 ... Metal body
- 4 ... Metallic foil object
- 5 ... Inorganic-dielectric thin film
- 6 ... Metal body
- 7 ... Electrode
- 8 ... aluminum 2O3 Substrate
- 9 ... Metallic foil object
- 10 ... Inorganic-dielectric thin film
- 11 ... Metal body
- 12 ... Polyimide insulator layer
- 13 ... nickel electrode
- 14 ... Solder bump
- 15 ... Semiconductor device

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#### CLAIMS

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[Claim(s)]

[Claim 1] The thin film capacitor characterized by providing a metallic foil object, the inorganic-dielectric thin film formed on the metallic foil object, and the metal body formed on the aforementioned inorganic-dielectric thin film.

[Claim 2] The thin film capacitor according to claim 1 characterized by carrying out at least one or more layer laminating membrane formation of an inorganic-dielectric thin film and the metal body, and involving in this metallic foil object on the aforementioned metallic foil object, or being folded up.

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[Translation done.]